Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A multi-level memory cell, comprising:
a substrate;
a gate disposed over the substrate;
a source region and a drain region configured in the substrate on each side of the gate; and
a bottom silicon oxide/silicon nitride/top silicon oxide layer disposed between the gate and the substrate, wherein the top silicon oxide has a first portion and a second portion from the direction of the source region to drain region, and the first portion has a thickness different from the second portion.

[c2] 2. The multi-level memory cell of claim 1, wherein the cell further comprises a pair of spacers disposed on each sidewall of the gate.

[c3] 3. The multi-level memory cell of claim 1, wherein the cell further comprises lightly doped regions disposed in the substrate underneath the spacers.

[c4] 4. The multi-level memory cell of claim 1, wherein material constituting the spacers comprises silicon oxide.

[c5] 5. The multi-level memory cell of claim 1, wherein the bottom silicon oxide layer has a thickness between about 20Å to 40Å.

[c6] 6. The multi-level memory cell of claim 1, wherein the silicon nitride layer has a thickness between about 40Å to 60Å.

[c7] 7. A multi-level memory cell, comprising:
a substrate;
a gate disposed on the substrate;
a source region and a drain region configured in the substrate on each side of the gate;
a tunneling dielectric layer disposed between the gate and the substrate;
a charge-trapping layer disposed between the tunneling dielectric layer and the gate; and
a top dielectric layer disposed between the charge-trapping layer and the gate, wherein the top dielectric layer has at least two portions from the direction of the source region to drain region, and each portion has different thickness.

[c8] 8. The multi-level memory cell of claim 7, wherein material constituting the charge-trapping layer comprises silicon nitride.

[c9] 9. The multi-level memory cell of claim 7, wherein the cell further comprises a pair of spacers disposed on each sidewall of the gate.

[c10] 10. The multi-level memory cell of claim 7, wherein the cell further comprises lightly doped regions configured in the substrate underneath the spacers.

[c11] 11. The multi-level memory cell of claim 7, wherein material constituting the spacers comprises silicon oxide.

[c12] 12. The multi-level memory cell of claim 7, wherein the tunneling dielectric layer has a thickness between about 20Å to 40Å.

[c13] 13. The multi-level memory cell of claim 7, wherein the charge-trapping layer has a thickness between about 40Å to 60Å.

[c14] 14. The multi-level memory cell of claim 7, wherein material constituting the tunneling dielectric layer comprises silicon oxide.

[c15] 15. The multi-level memory cell of claim 7, wherein material constituting the top dielectric layer comprises silicon oxide.